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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/593,668	05/01/2007	Neil Buxton	3711-000121/US/NP	2798

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EXAMINER	
ROCHE, JOHN B	
ART UNIT	PAPER NUMBER
2184	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/593,668	BUXTON ET AL.	
	Examiner	Art Unit	
	JOHN B. ROCHE	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 23, 2009 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-7, 9-13 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Microsoft Device Driver for Symbios Logic ATA/ATAPI-to-1394 Controller Included in Microsoft's New NT5 Beta DDK Release, 10/6/1997," hereafter

referred to as Microsoft'997, in view of Harris et al. (US 2002/0081873), hereafter referred to as Harris'873.

Referring to claim 7, Microsoft'997 teaches a host apparatus arranged to transmit commands to an external storage medium device connected to the host apparatus over an external databus which is arranged in accordance with one of the IEEE 1394 standard and the Universal Serial Bus standard, the host apparatus comprising: a command bus and a command interface arranged in accordance with one of the ATA/IDE standard and the Serial ATA standard for transmitting commands to a storage medium device over the command bus (ATA commands transmitted through 1394-to-ATA bridge via SBP-2 protocol, paragraph 3, lines 2-5); and at least one integrated circuit chip connected to the command bus and having terminals for connection to the external databus (SYM13FW500 ATA/ATAPI-to-1394 controller, paragraph 1, line 1); and to supply the converted commands to the terminals for connection to the external databus (controller contains capability for an external PHY, paragraph 4, lines 6-7).

Microsoft'997 does not appear to explicitly teach the integrated circuit chip having an interface arranged to convert commands received from the command bus in a format in accordance with one of the ATA/IDE standard and the Serial ATA standard

into a format in accordance with said one of the IEEE 1394 standard and the Universal Serial Bus standard; rather, it teaches conversion in the opposite direction (1394-to-ATA bridge, paragraph 3, line 5).

However, Harris'873 teaches an integrated circuit chip (bridging chip 100 as seen in figure 2 and paragraph 16, lines 5-6) having an interface (bridging chip provides bridging circuit, paragraph 16, lines 5-6) arranged to convert commands received from the command bus in a format in accordance with one of the ATA/IDE standard and the Serial ATA standard (ATA/ATAPI signals, paragraph 16, line 3) into a format in accordance with said one of the IEEE 1394 standard and the Universal Serial Bus standard (USB signals, paragraph 16, lines 4-5).

Microsoft'997 and Harris'873 are analogous art because they are both drawn to the same field of endeavor of the conversion of data from one protocol to another.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Microsoft'997 and Harris'873 before him or her, to modify Microsoft'997's integrated circuit chip to include an interface arranged to convert commands received from the command bus in a format in accordance with one of the ATA/IDE standard and the Serial ATA standard into a format in accordance with said one of

the IEEE 1394 standard and the Universal Serial Bus standard, as taught in Harris'873, because conversion between protocols is well understood in the art.

The motivation to combine these teachings would have been to enable mass storage applications to benefit from the speed and versatility of the USB protocol (paragraph 5, lines 2-4).

Therefore, it would have been obvious to combine the teachings of Microsoft'997 and Harris'873 to bring about the invention as claimed above.

4. Note that 1 and 13 contain the corresponding limitations of claim 7 as shown above; therefore, they are rejected using the same reasoning accordingly.

5. As to claim 9, Microsoft'997 anticipates a host apparatus according to claim 7, wherein said one of the ATA/IDE standard and the Serial ATA standard is the ATA/IDE standard (ATA device, paragraph 3, line 4).

6. Note that claims 3 and 15 contain the corresponding limitations of claim 9 as shown above; therefore, they are rejected using the same reasoning accordingly.

7. As to claim 10, Microsoft'997 anticipates a host apparatus according to claim 7, wherein said one of the IEEE 1394 standard and the Universal Serial Bus standard is the IEEE 1394 standard (1394 command sets, paragraph 3, lines 2-3).

8. Note that claims 4 and 16 contain the corresponding limitations of claim 10 as shown above; therefore, they are rejected using the same reasoning accordingly.

9. As to claim 11, Microsoft'997 anticipates a host apparatus according to claim 10, wherein said one of the IEEE 1394 standard and the Universal Serial Bus standard is the IEEE 1394 standard including a Serial Bus Protocol (SBP-2, paragraph 3, line 1).

10. Note that claims 5 and 17 contain the corresponding limitations of claim 11 as shown above; therefore, they are rejected using the same reasoning accordingly.

11. As to claim 12, Microsoft'997 anticipates a host apparatus according to claim 7, wherein the interface of the integrated circuit chip comprises: a first layer arranged in accordance with said one of the ATA/IDE standard and the Serial ATA standard to receive commands from the command bus (ATA device,

paragraph 3, line 4); a second layer arranged to convert commands output from the first layer into a format in accordance with said one of the IEEE 1394 standard and the Universal Serial Bus standard (1394-to-ATA bridge, paragraph 3, line 5); and a third layer arranged in accordance with said one of the IEEE 1394 standard and the Universal Serial Bus standard to transmit the converted commands over the external databus (SBP-2 protocol embedded in the controller, paragraph 3, lines 1-2).

12. Note that claims 6 and 18 contain the corresponding limitations of claim 12 as shown above; therefore, they are rejected using the same reasoning accordingly.

13. Claims 2, 8 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Microsoft'997 in view of Harris'873 as applied to claim 7 above, and further in view of Hatano (US 2002/0002645), hereafter referred to as Hatano'645.

14. As to claim 8, Microsoft'997 does not appear to explicitly teach a host apparatus according to claim 7, wherein the host apparatus is a digital television receiver apparatus.

However, Hatano'645 teaches the host apparatus according to claim 7, wherein the host apparatus is a digital television

receiver apparatus (1394 bus may couple a digital broadcast receiving device and a digital television, paragraph 5, lines 5-7).

Microsoft'997 and Hatano'645 are analogous because they are both drawn to the same inventive area of conversion between interface protocols.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Microsoft'997's system to incorporate, as taught by Hatano'645, the host apparatus according to claim 7, wherein the host apparatus is a digital television receiver apparatus because in such devices conversion between signal interface protocols is common, such as in "digital cable" boxes that are connected to analog televisions.

The motivation to combine these teachings would have been to provide reliable communication and control among electronic devices coupled through different types of interfaces (paragraph 15, lines 1-4).

Therefore, it would have been obvious to combine the teachings of Microsoft'997 with the teachings of Hatano'645 to bring about the invention as claimed above.

15. Note that claims 2 and 14 contain the corresponding limitations of claim 8 as shown above; therefore, they are rejected using the same reasoning accordingly.

Response to Arguments

16. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Referring to independent claims 1, 7 and 13, Applicant argues that "Microsoft'997 does not set forth 'each and every element' of the independent claims of the present application 'in as complete detail as is contained in the… claim' (page 3, lines 7-8)." Applicant specifically pointed out the failure of Microsoft'997 to teach or suggest converting commands in the ATA/IDE or SATA protocols into commands in the IEEE1394 or USB protocols (page 2, lines 14-17).

Examiner respectfully submits that while Microsoft'997 does not appear to explicitly teach this particular component of the invention as claimed above, the bridging chip in Harris'873 teaches this component, as shown above.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN B. ROCHE whose telephone number is (571)270-1721. The examiner can normally be reached on 8:30 am - 5:00 pm, M-F EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Henry Tsai can be reached on 571-272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JR

/Henry W.H. Tsai/
Supervisory Patent Examiner, Art Unit 2184